High κ dielectrics on high carrier mobility InGaAs compound semiconductors and GaN - Growth, interfacial structural studies, and surface Fermi level unpinning

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The semiconductor industry is now facing unprecedented challenges in materials and physics due to the limitations of Si CMOS transistor scaling arising from nonscaling of matters, namely gate dielectrics and channel mobilities. The drive for alternative high κ dielectrics (for replacing SiO_2) and metal gates initiated a decade ago has resulted in a recent ***Intel's news announcement of high κ + metal gate transistor breakthrough on 45 nm microprocessors,*** indeed a scientific and technological achievement. However, even with very aggressive adoption of new methods for performance enhancements, the industry may have run out of technologies. As driven by continual demands of faster speed of enhanced transport in channels and reducing power dissipation beyond the 16 nm node, to extend the Moore's Law, the current consensus is that we urgently need to employ III-V InGaAs compound semiconductors as high electron mobility channels integrated with high κ gate dielectrics for future CMOS technology. The realization of these new MOSFET's has posted great tasks not only for ***material scientists*** and ***processing engineers***, but also for ***condensed matter*** and ***device physicists as a whole***.

We have achieved many firsts in this important nano-electronics research, critical for electronic industry technologies in the present 32-22 nm node and beyond Si CMOS: the following four items are our report with the detailed listed in the next few pages.

(1) First to achieve full Fermi level unpinning in oxide-$In_{0.2}Ga_{0.8}As$, a must for fabricating inversion-channel MOSFET.
(2) First to perform *in-situ* XPS analysis to determine the energy-band parameters at interfaces of high κ ALD oxides on GaAs and InGaAs, and showed that absence of arsenic oxide and elemental arsenic was a principal mechanism responsible for Fermi level unpinning at the dielectric oxide/GaAs interface, thereby leading to effective passivation of the GaAs and InGaAs surfaces. ALD has been widely used in the Si industry for high k gate dielectrics deposition.
(3) First to demonstrate oxide scaling of MBE-grown GGO on $In_{0.2}Ga_{0.8}As$ to a CET of 1.0 nm and high-temperature thermal stability withstanding 850°C RTA, critical for inversion- channel III-V MOSFETs.
(4) First to achieve inversion-channel GaN nMOSFET with atomic-layer-deposited Al_2O_3 as gate dielectric.

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14. ABSTRACT
This is a project on nano-electronics, which achieved many firsts: full Fermi level unpinning in oxide-In0.2Ga0.8As, determined energy-band parameters at interfaces of high κ atomic-layer-deposited (ALD) oxides on GaAs and InGaAs, and first to achieve inversion-channel GaN on MOSFET with ALD Al2O3 as gate dielectric.

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CMOS, Gallium Nitride , Nanotechnology

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1 Fermi level unpinning in oxide-$In_{0.2}Ga_{0.8}As$

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The drive for technologies beyond the 22-16nm node CMOS has demanded the integration of high-mobility channels such as InGaAs with high κ gate dielectrics. Consequently, the III-V MOS transistors need to be operated with their oxide- III-V interfaces resembling that of SiO_2-Si, namely nearly perfect passivation. Through the charge trapping characteristics, *C-V* measurements under wide range of temperatures are required to fully characterize the interfacial trap density (D_{it}) distribution inside the whole range of the energy gap of III-V MOS system. The passivation of the III-V InGaAs interfaces, therefore, needs to be measured, qualified, and quantified not only by the conventional methods, but also by the ones taking the III-V's bandgap and trapping properties into account. Recent inversion-channel $In_{0.53}G_{0.47}As$ MOSFET's have shown very impressive device results, in terms of drain currents and trans- conductance. For the lower In-content InGaAs such as $In_{0.2}Ga_{0.8}As$, inversion-channel devices have not fared as well. In this work, we have, therefore, focused on $In_{0.2}Ga_{0.8}As$, but the measurements and methodology are readily applied to other InGaAs systems.

(I) *C-V* characteristics under light illumination

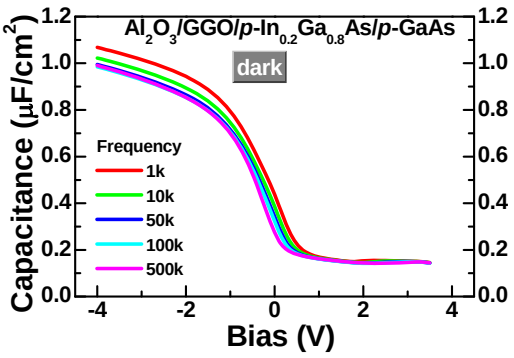
Well behaved *C-V* characteristics taken in the dark show small frequency dispersion and no visible distortion in *C-V* curves, a typical signature of an insignificant interfacial density of states. The small frequency dispersion indicates superior quality in both the oxide-InGaAs interface and the strained $In_{0.2}Ga_{0.8}As$ layer. However, no inversion due to thermal generation/recombination was observed in our *C–V* measurements even at very low sweep rates. This was ascribed to the lower generation rate of minority carriers in $In_{0.2}Ga_{0.8}$ As/GaAs structures. High optical generation rates for electrons and holes, however, can be readily achieved with low-intensity light illumination, resulting in clear carrier accumulation and inversion. The measured *C-V* characteristics with almost all frequencies (50 Hz-500 kHz) tightened up together may be the best among all work reported for high-k dielectrics on the III-V's. The excellent inversion behavior of *p*-$In_{0.2}Ga_{0.8}As$/GaAs demonstrated was also unprecedented in high-κ dielectrics/*p*-$In_{0.2}Ga_{0.8}As$, demonstrating free Fermi-level movement near the conduction band edge. An atomically smooth, sharp oxide/InGaAs interface after high-temperature annealing has been achieved, indicating the thermal stability of Al_2O_3/GGO/$In_{0.2}Ga_{0.8}As$.

(II) *C-V*/*G-V* characteristics under various temperatures

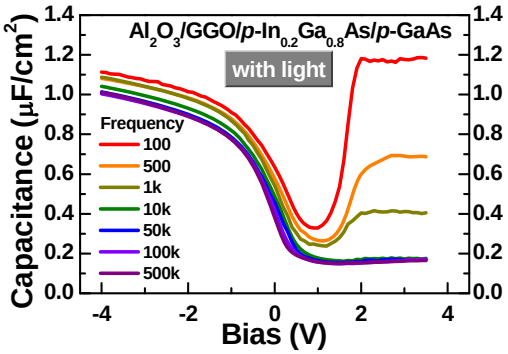
The measurement windows for $In_{0.2}Ga_{0.8}As$ under different temperatures according to charge trapping characteristics were calculated. Avery small frequency dispersion at accumulation at room and low temperature indicates low D_{it} for most of the upper bandgap. A low D_{it} within the measurement window at room temperature can also be concluded.

From the conductance (*G-V*) spectroscopy maps, unobstructed Fermi-level movement was observed in the upper and lower 1/3 of the bandgap. In these regions, steep Fermi-level traces with respect to gate bias reveal high modulation efficiency, low electrical friction at the GGO/$In_{0.2}Ga_{0.8}As$ interface and low D_{it}'s. High temperature *C-V*'s at 150°C indicates minority carrier traps near mid-gap region for both n and p type samples. Similar conclusion can be drawn from the corresponding conductance maps. The decreasing slopes of Fermi-level movement with respect to bias also confirm the trapping of the carriers and an increase in friction against gate modulation near the mid-bandgap. It appears that higher inversion bias is required to move the Fermi-level beyond this region to achieve strong inversion. High temperature *C-V* and *G-V* results show signs of high interface traps around midgap, as revealed by the *C-V* bumps in the inversion region, as well as the increasing friction against gate modulation seen near the same region.

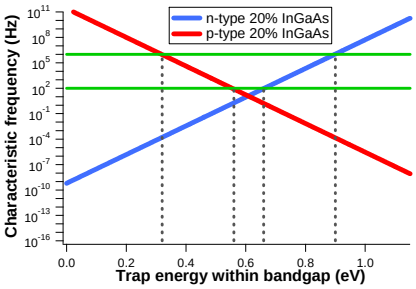
C-V measurements under light illumination and under wide range of temperatures have been performed on UHV- deposited Al_2O_3(3nm)/Ga_2O_3(Gd_2O_3)(8.5nm) on n- and p-$In_{0.2}Ga_{0.8}As$/GaAs. The results exhibit very high-quality interface and free-moving Fermi-level near the band-edges (regions close to E_c and E_v), setting a new benchmark for III-V InGaAs passivation.



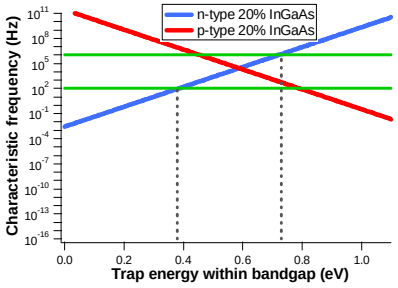
C-V characteristics of sample A measured from 1 kHz to 500 kHz in the dark with almost all frequencies tightened up together.



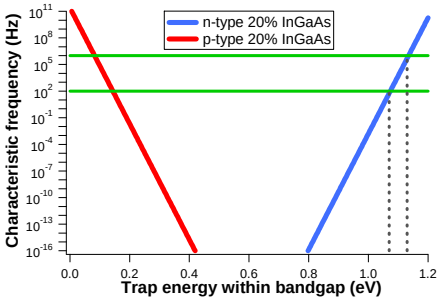
C-V characteristics of sample A measured under light illumination, demonstrating the excellent inversion behavior in high-κ dielectrics/III-V's and free moving Fermi-level near both the conduction and valence band edges.



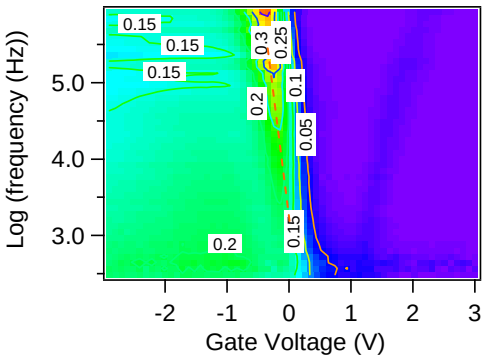
Charge trapping characteristics for *n*-type and *p*-type $In_{0.2}Ga_{0.8}As$ at 25°C. Traps visible to the measurement from 100Hz to 1MHz have energy levels between the dash lines.



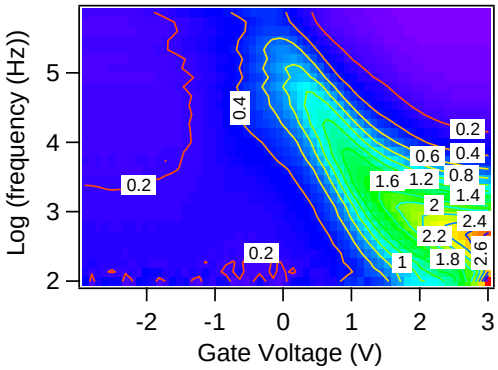
Charge trapping characteristics for *n*-type and *p*-type $In_{0.2}Ga_{0.8}As$ at 150°C and corresponding measurement window with 100 Hz to 1 MHz *C-V* measurement frequency.



Charge trapping characteristics for *n*-type and *p*-type $In_{0.2}Ga_{0.8}As$ at 77K and corresponding measurement window with 100 Hz to 1 MHz *C-V* measurement frequency.



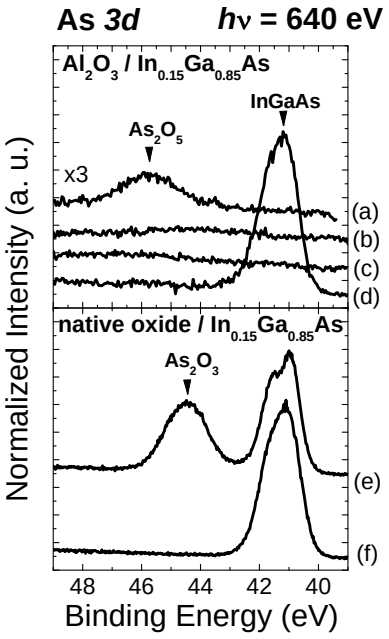
G-V characteristics of sample A measured from 100 Hz to 1 MHz under room temperature. Steep Fermi-level trace indicates high modulation efficiency with respect to gate bias which is the evidence of a low D_{it}.



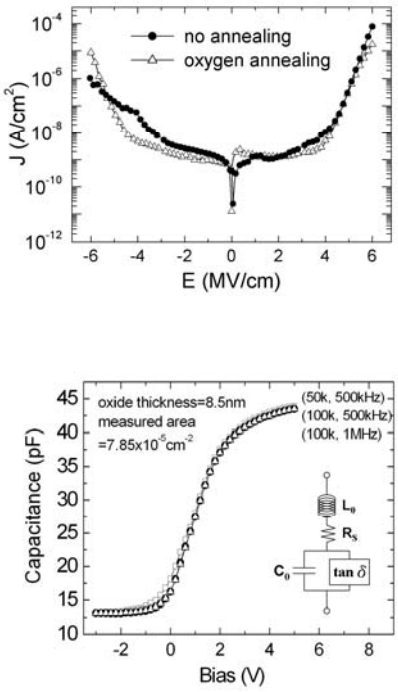
G-V characteristics of sample A measured from 100 Hz to 1 MHz at 150°C. Fermi-level trace slope decreases as MOS biased into the inversion region. An increase of traps near mid-bandgap is concluded.

2-1. Surface passivation of III-V InGaAs compound semiconductors using ALD-Al_2O_3

Al_2O_3 was deposited on $In_{0.15}Ga_{0.85}As$/GaAs using atomic layer deposition (ALD). Without any surface preparation or post thermal treatment, excellent electrical properties of Al_2O_3/InGaAs heterostructures were obtained, in terms of low electrical leakage current density (10^{-8} to 10^{-9} A/cm^2) and low interfacial density of states (D_{it}) in the range of 10^{12} cm^{-2}eV^{-1}. The interfacial reaction and structural properties were studied by high-resolution x-ray photoelectron spectroscopy and high-resolution transmission electron microscopy. The depth profile of HR-XPS, using synchrotron radiation beam and low energy Ar^+ sputtering, exhibited no residual arsenic oxides at interface. The removal of the arsenic oxides from Al_2O_3/InGaAs heterostructures during ALD process ensures the Fermi level unpinning, which was observed in the C-V measurements. The HR-TEM shows sharp transition from amorphous oxide to single crystalline semiconductor.



As 3*d* core level spectra recorded from two samples, $Al_2O_3/In_{0.15}Ga_{0.85}As$ (InGaAs) (top) and native oxide/InGaAs (bottom): (a) at the surface of Al_2O_3; (b) immediately below the Al_2O_3 surface; (c) in the bulk of Al_2O_3; (d) at the interface of Al_2O_3/InGaAs; (e) at the surface of air- exposed InGaAs; and (f) in the bulk of InGaAs

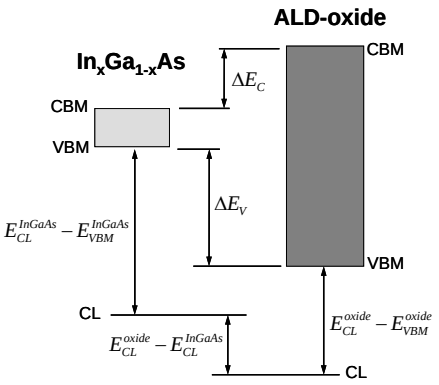


(a) Leakage current density J (A/cm^2) vs E (MV/cm) for $Al_2O_3/In_{0.15}Ga_{0.85}As$ hetero-structure in different thermal processes, (b) C-V curves of Au/Al_2O_3(8.5nm)/$In_{0.15}Ga_{0.85}As$.

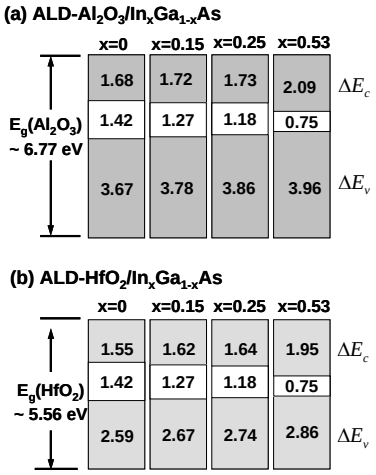
2-2. Energy parameters and surface passivation of ALD-Al_2O_3 and HfO_2/III-V $In_xGa_{1-x}As$

III-V $In_xGa_{1-x}As$ metal-oxide-semiconductor field-effect-transistors (MOSFETs) with high κ dielectrics are now a strong contender for technologies beyond the 22-16 nm node complementary MOS (CMOS), due to the high electron mobility of $In_xGa_{1-x}As$ (x = 0 to 1) 6 - 18 times of that of Si. Low interfacial densities of states (D_{it}'s) of less than ~10^{12} eV^{-1}cm^{-2}, small frequency dispersion, and low electrical leakage currents of 10^{-8} A/cm^2, with unpinned surface Fermi level, similar to those exhibited in the traditional SiO_2/Si, are required for the high κ dielectrics on InGaAs. These properties have been attained in ultra high vacuum (UHV) deposited high κ $Ga_2O_3(Gd_2O_3)$ [GGO] and Gd_2O_3 on InGaAs, without an interfacial layer. $In_xGa_{1-x}As$ MOSFETs have been successfully demonstrated with excellent device characteristics. A capacitive effective thickness (CET) value of 1.0 nm has also been achieved in ALD-HfO_2 on $In_{0.53}Ga_{0.47}As$/InP. Note that the CET is simply the thickness that is derived directly from the relationship of CET(V) = (κ_{SiO2})*(ε_0)*(Area)/C(V), where ε_0 is the permittivity of free space, and C(V) is the measured capacitance at a biasing voltage V. Furthermore, high temperature stability of 850 ^oC has been achieved in Al_2O_3/GGO/InGaAs.

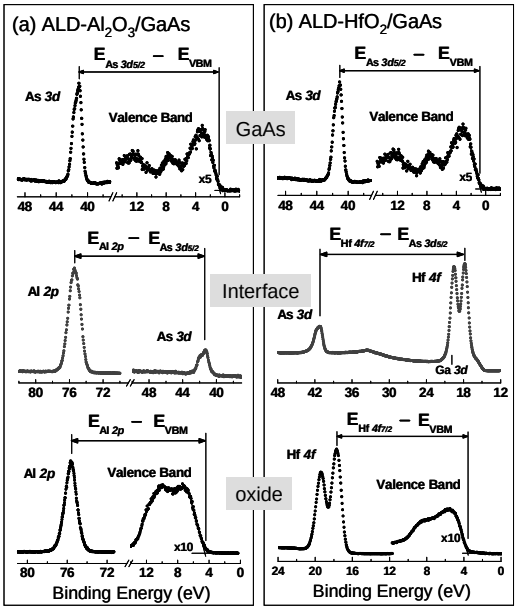
In addition to low D_{it}, small leakage currents, and device characteristics, energy-band parameters of high κ gate dielectrics/InGaAs, including oxide energy-band gaps (E_g), conduction-band offsets (ΔE_c) and valence-band offsets (ΔE_v), are essential for studying MOS device physics, design, and modeling. X-ray photoelectron spectroscopy (XPS) combined with reflection electron energy loss spectroscopy (REELS) were used to determine the energy-band parameters, valence-band offsets ΔE_V, conductance-band offsets ΔE_V, and energy-band gaps E_g, of the atomic layer deposited (ALD) Al_2O_3 and HfO_2 on $In_xGa_{1-x}As$ (x=0, 0.15, 0.25, and 0.53). Using REELS, E_g values of the ALD-Al_2O_3 and -HfO_2 were estimated to be 6.77 and 5.56 ±0.05 eV, respectively. The ΔE_V's were determined by measuring the core-level to valence band maximum binding energy difference from the XPS spectra. The ΔE_C's were then extracted from ΔE_V's and the energy band gaps of the oxides and $In_xGa_{1-x}As$, and are in good agreement with those estimated from the Fowler-Nordheim tunneling. The ΔE_C's and ΔE_V's are larger than 1.5 and 2.5 eV, respectively, for all the ALD-oxide/$In_xGa_{1-x}As$ samples.



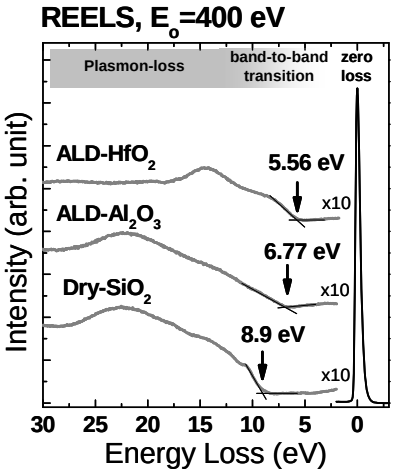
Schematic illustration of the energy band lineup at ALD-oxide/InGaAs interface.



Energy band parameters for (a) $Al_2O_3/In_xGa_{1-x}As$ and (b) $HfO_2/In_xGa_{1-x}As$ hetero-structures acquired by using HR-XPS and REELS.



XPS spectra of (a) As *3d* core level and valence band of GaAs film, Al *2p* and As *3d* core levels at the ALD-Al_2O_3/GaAs interface and Al *2p* core level and valence band of Al_2O_3 film (b) As *3d* core level and valence band of GaAs film, Hf *4f* and As *3d* core levels at the ALD-HfO_2/ GaAs interface and Hf *4f* core level and valence band of HfO_2 film.

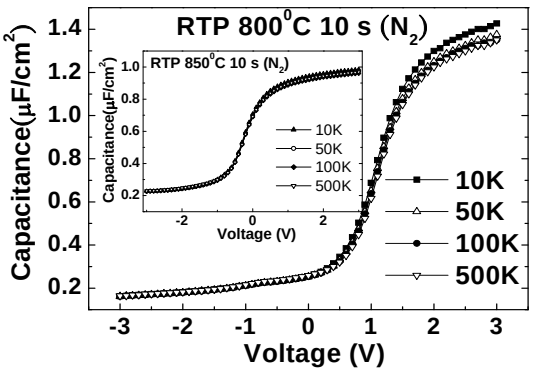


Reflection electron energy loss spectra for ALD-HfO_2, ALD-Al_2O_3 and SiO_2 thin films at the primary energy of 400 eV.

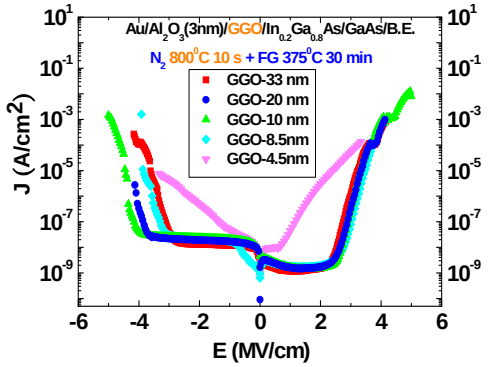
3. Achieving 1 nm CET in MBE-$Ga_2O_3(Gd_2O_3)$/$In_{0.2}Ga_{0.8}As$ and high temperature (850°C) stability

Scaling high κ oxides to nanometer range as well as unpinning surface Fermi level of the III-V semiconductors has been one main focus of recent high κ research on high mobility channel materials. Previously, we discovered that $Ga_2O_3(Gd_2O_3)$ [GGO] ultra high vacuum (UHV) deposited on III-V's of GaAs and InGaAs has unpinned surface Fermi level, and showed low interfacial state density. Inversion-channel and depletion-mode metal-oxide-semiconductor field-effect-transistors (MOSFET's) employing GGO as the gate dielectric were demonstrated. Due to the tendency of GGO to absorb moisture upon air exposure leading to degradations of electrical performance, relatively thick oxides in the range of 25-55 nm were used in the earlier studies of MOS capacitors and transistors to minimize the moisture-absorption effects. Post annealing under UHV or flowing nitrogen gas of thick air-exposed GGO was shown to expel moisture, thus restoring low interfacial density of states (D_{it}), low leakage currents and maintaining smooth oxide-semiconductor interfaces. However, very little work has been reported on scaling of capacitive effective thickness (CET) of GGO to 1 nm due to degraded oxide/ III-V interfaces caused by air-exposure, which may not be recovered upon UHV annealing, in contrast to thicker GGO films. Here CET is defined as $\kappa_{SiO2} \times t_{high\ \kappa} / \kappa_{high\ \kappa}$.

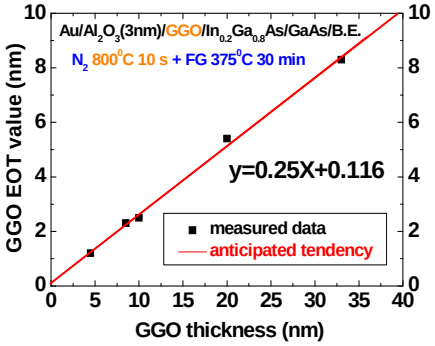
We demonstrate the GGO scaling approaching 1 nm CET in GGO/$In_{0.2}Ga_{0.8}As$ gate stack with aid of an *in-situ* deposited Al_2O_3 3 nm thick on top of GGO, which serves as a protection layer owing to its thermal and chemical stabilities against moisture. MOS capacitors with the dual-dielectric layer on InGaAs were also shown to withstand rapid-thermal-annealed (RTA) to 800-850°C. Excellent capacitance-voltage (*C-V*) characteristics in terms of small flat-band voltage, a small frequency dispersion of measured capacitances at accumulation, and D_{it}'s in the low 10^{11} $cm^{-2}eV^{-1}$ have been achieved. Moreover, the κ values of GGO remaining around 14-16 are obtained for all GGO thicknesses ranging from 33, 20, 10, 8.5, to 4.5 nm (with κ values of 3 nm Al_2O_3 estimated to be 9-7). The smallest EOT of GGO achieved in this work is 1.25-1.1 nm, along with low leakage current densities of 3.1×10^{-5} and 2.5×10^{-9} A/cm^2 at biasing voltage of V_{fb} + 1V for GGO films of 4.5 and 8.5 nm, respectively.



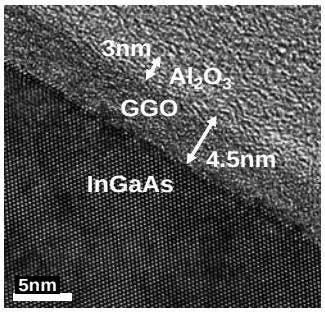
C-V characteristics for an Al_2O_3(3nm)/GGO(4.5nm)/$In_{0.2}Ga_{0.8}As$/ GaAs MOS diode RTA to 800°C with the Au gate deposited afterwards. The inset shows C-V characteristics of another 8.5 nm sample, which was RTA to 850°C with the Al gate. The capacitor area is 7.85 x 10^{-5} cm^2.



Comparison of *J-E* characteristics among all tested samples for GGO scalability issue



Scalability relationships between GGO thickness and EOT value



Cross-sectional HR-TEM image of the 4.5 nm sample after RTA 800°C-850°C 10s under N_2

Table I. Summary of GGO scalability and relevant electrical properties, including GGO dielectric constant (κ), flat-band voltage (V_{fb}), frequency dispersion of capacitance at accumulation, leakage current density at $V_g = V_{fb} + 1V$, interfacial density of states (D_{it}) near the mid-gap, and GGO CET values.

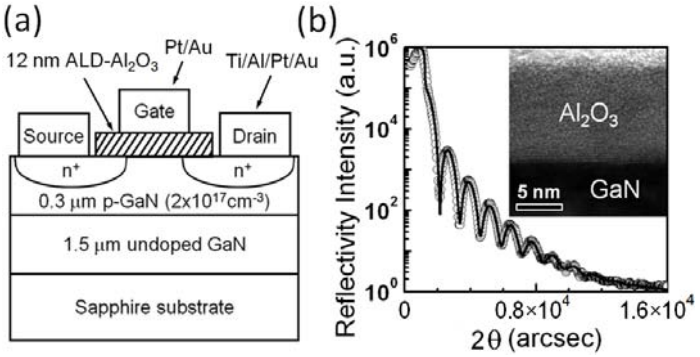
Au gate metal (RTA 800°C 10s)						
GGO thickness	**GGO κ value**	**V_{fb}**	**Dispersion (10k-500kHz)**	**J@V_{fb}+1V (A/cm^2)**	**D_{it} (10^{11} cm^{-2}eV^{-1})**	**GGO CET (nm)**
33 nm	**15-16**	**3.5V**	**2.8%**	**1.18×10^{-9}**	**1.3**	**8.6-8.0**
20 nm	**14-15**	**1.3V**	**1.5%**	**1.62×10^{-9}**	**1**	**5.6-5.2**
10 nm	**14-15**	**1.1V**	**2.2%**	**1.46×10^{-9}**	**1.4**	**2.8-2.6**
8.5 nm	**14-16**	**1.1V**	**4.7%**	**1.78×10^{-9}**	**2.6**	**2.4-2.1**
4.5 nm	**14-16**	**1.1V**	**5.4%**	**3.1×10^{-5}**	**1.3**	**1.3-1.1**
Al gate metal (RTA 850°C 10s)						
8.5 nm	**14-16**	**0.1V**	**2.6%**	**2.5×10^{-9}**	**2.5**	**2.4-2.1**

Note that D_{it}s' near the mid-gap were measured using the high frequency conductance method. Very small flat-band voltage shifts of 0.1-0.3 eV were measured, again indicating small D_{it}s'.

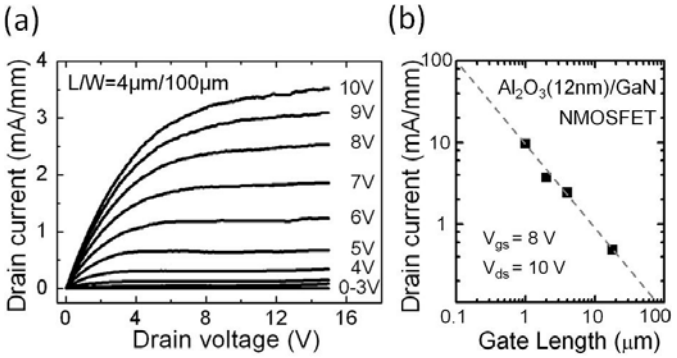
4. Inversion-channel GaN nMOSFET with atomic-layer-deposited Al_2O_3 as gate dielectric

GaN, with a high saturation velocity at high electrical fields (υ_{sat} ~ 3×10^7 cm/s at 150 kV/cm), a high critical electrical field (up to 3 MV/cm), good thermal conductivity, and epi-layers grown on Si, has been widely studied for applications in high-power and high-temperature devices such as hetero-junction field-effect-transistors (HFETs). Compared to conventional RF AlGaN/GaN HFETs, GaN metal-oxide-semiconductor field-effect- transistors (MOSFETs) feature a larger voltage sweep range, lower gate leakage currents and circuit simplicity, and hence have attracted much interest lately. Owing to its wider energy band gap (3.4 eV) which alleviates the adverse affects like drain-induced barrier lowering (DIBL) and band-to-band tunneling (BTBT), GaN is now also being considered as a channel candidate for the next generation complementary metal-oxide- semiconductor (CMOS) devices beyond the 22nm node technology. Furthermore, by taking into account of the short channel effect with the cutoff frequency (f_T) given by $f_T=\upsilon_{sat}/2\pi L$ (where L is the gate length), GaN MOSFET's may outperform its counterparts of Si and GaAs in further scaled-down devices, despite the fact that GaN offers no special advantage in electron mobility.

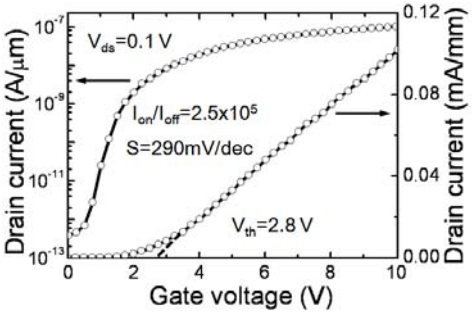
Inversion n-channel GaN metal-oxide-semiconductor field-effect-transistors (MOSFETs) using atomic-layer-deposited (ALD) Al_2O_3 as a gate dielectric have been successfully fabricated, showing well-behaved drain *I-V* characteristics. The drain current was scaled with gate length (varying from 1 to 16μm), showing a maximum drain current of ~10 mA/mm in a device of 1 μm gate length, at a gate voltage of 8 V and a drain voltage of 10 V. At drain voltage of 0.1 V, a high I_{on}/I_{off} ratio of 2.5×10^5 was achieved with a very low off-state leakage of $4\text{x}10^{-13}$ A/μm. Both MOSFET and MOS capacitor showed very low leakage current densities of 10^{-8} A/cm^2 at biasing fields of 4MV/cm. The interfacial density of states (D_{it}) was calculated to be $(4\text{-}9)\times10^{11}$ cm^{-2} eV^{-1} near the midgap.



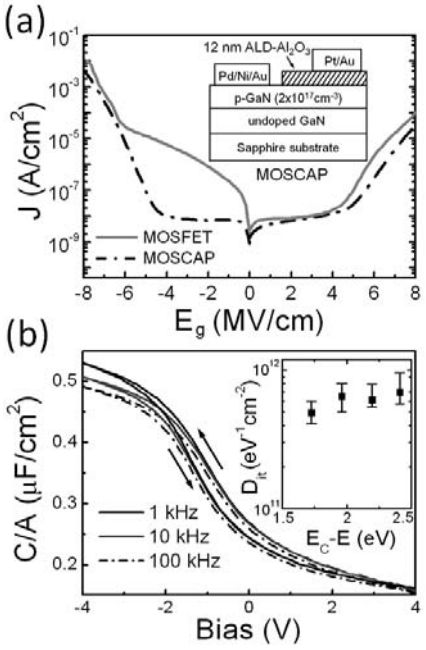
A schematic view of the inversion-channel GaN MOSFET with ALD-Al_2O_3 as gate dielectric; (b) cross-sectional HR-TEM image and low angle XRR of Al_2O_3 on GaN, with experimental data (dots) and a theoretical fit (line)



(a) Drain *I-V* characteristic for a 4 μm gate length GaN MOSFET; (b) the scaling characteristic of drain current versus gate length



Transfer characteristics for a 4 μm gate length GaN MOSFET at a drain voltage V_{ds} of 0.1 V.



(a) Leakage current density (*J*) vs gate electrical field (E_g) for Al_2O_3/GaN MOSCAP and MOSFET, with the inset showing schematic view of the GaN MOSCAP; (b) *C-V* curves for the MOSCAP under frequencies varying from 1 kHz to 100 kHz, with the inset showing D_{it} values calculated by the conductance method.